UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,421	10/20/2003	Denny D. Tang	TS02-818	2802

7590 02/08/2005

STEPHEN B. ACKERMAN
28 DAVIS AVENUE
POUGHKEEPSIE, NY 12603

EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,421	TANG ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/29/04, 4/15/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: search history.

DETAILED ACTION

Information Disclosure Statement

1. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 29 January 2004 and 15 April 2004. The information disclosed therein was considered.

Specification

2. Claims 10, 14, 18, 22, 26 and 30 are objected to because of the following informalities:

Claims 10 and 18 appear to contain a typographical error; namely, "restive" should be --resistive--.

Claims 14 and 22 appear to have a dependency error; namely, claims 14 should depend on claim 12, and claim 22 should depend on claim 20, since both claims 14 and 22 recite "the first and second mirrored replication currents" which has an antecedent basis in claims 12 and 20, respectively (instead of claims 13 and 21). Also, see claim 6 which has a similar dependency.

Claim 26 recites "each multilevel magnetic tunneling junction". It is unclear whether it is referring to that of the array or of the reference generator. In view of claim 30, it will be understood as that of the array, and it is suggested that --within said array-- be inserted in claim 26 in a manner similar to that of claim 30 to clarify the claimed subject matter.

Claim 26 (as understood per the objection above) and claim 30 appear to lack support in the specification or in the figures, since the plurality of multilevel magnetic tunneling junctions of the reference generator seem to be disclosed as replicas of those of the array, and therefore

each junction within the array would have a resistance substantially equal to the resistance of one of the junctions within the reference generators. In view of Fig. 4, these claims will be understood as each array junction having a resultant current level different from each of the plurality of reference current levels.

Appropriate corrections are required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al. (U.S. Pat. No. 6,317,376) in view of Takai (Japanese Patent JP 62293327 A).

Regarding claim 1, Tran, for example in Fig. 1, discloses a reference generator for providing a reference level, comprising: a first nonlinear resistive element (for example, 104 in 110) biased at a constant level (Vs) to impart first resultant level (Ira) from said first resistive element; a second nonlinear element (for example, 104 in 112) biased at the constant level (Vs) to impart second resultant level (Irb) from said second resistive element; and a reference level combining circuit (including 126) connected to receive the first resultant level and the second resultant level, from a combination of the first resultant level and the second resultant level creates the reference level (the combination of Ira and Irb inputted to 126).

However, Tran does not disclose a first and a second mirror sources respectively in communication with the first and the second nonlinear resistive elements to receive the first and the second resultant levels and provide a first and a second mirrored replications of said first and said second resultant levels to the reference level combining circuit (instead of the first and second resultant levels).

Takai, for example in Fig. 1, discloses a first mirror source (including 1 and 3) in communication with a first resistive element (20) to receive a first resultant level (a current through 20) and provide a first mirrored replication (through 3) of said first resultant level, and a second mirror source (including 4 and 5) in communication with a second resistive element (21) to receive a second resultant level (a current through 21) and provide a second mirrored replication (through 4) of said second resultant level, wherein the first and the second mirrored replications, which represent currents with different characteristics, are combined (at the intersection of 3 and 4).

Since use of current mirrors as current sources was common and well known in the art (as exemplified by Takai), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to include current mirrors (as in Takai) in the reference generator of Tran to provide the reference currents, for the purpose of generating more stable and reliable reference currents indicative of the states of the reference cells.

Regarding claims 2-4 and 6-8, the above Tran/Takai combination further discloses that the first resistive element has a resistance different from the resistance of the second resistive

element (corresponding to logic values '0' and '1', respectively; see for example column 3, lines 19-38);

that the first and second resistive elements are multilevel (2 levels) magnetic tunnel junctions set to differing parallel and anti-parallel magnetic orientations (see for example column 3, line 10-38);

that the constant level is a constant voltage (Vs) and the first and second resultant levels are currents (Ira and Irb);

that the reference level combining circuit comprises: a current summing circuit to additively combine the first and second resultant currents (at the intersection of 128 and 130), and a current scaling circuit (including the half-gain amplifier 126) to create a scaling of the combined first and second resultant current to create a reference current (which is half of the sum of Ira and Irb; see for example column 4, lines 33-39);

that the reference level is the reference current (related to the reference voltage Vref via the feedback reference Rf; see column 4, lines 33-39);

and a reference resistor (Rf) associated with the reference level combining circuit to receive the reference current wherein the reference level is a voltage developed across the reference resistor with said reference current flowing through the reference resistor (see for example column 4, lines 33-39).

Regarding claim 5, the above Tran/Takai combination discloses a reference generator as in claim 1, with the exception of the first and second resultant levels and the first and second mirrored replications being voltages. It would have been obvious at the time the invention was

made to a person having ordinary skill in the art to convert the current levels to voltages for summing, scaling, monitoring, etc., since converting currents to voltages for such functions was common and well known in the art.

5. Claims 9-32, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Tran et al. (U.S. Pat. No. 6,317,376) in view of Takai (Japanese Patent JP 62293327 A) as applied to claims 1-8 above, and further in view of Naji (U.S. Pat. No. 6,169,689).

The above Tran/Takai combination discloses a reference generator as in claims 1-8, and a related method, with the exception of a plurality of the reference level combining circuits for a multilevel magnetic random access memory.

Naji discloses a multilevel magnetic random access memory (Fig. 2) with a plurality of reference levels (VR1, VR2 and VR3 in Fig. 4; see also column 3, line 37 through column 4, line 33).

Since Naji discloses the reference levels being respectively related to intermediate resistance values between every adjacent two of the multiple resistance values of each memory cell (see for example column 4, lines 1-33), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the sensing means of the Tran/Takai combination to the multilevel memory of Naji, by providing a plurality of multilevel reference cells set to respective resistance values of the multilevel memory cell, and a plurality of the reference level combining circuits similar to that of the Tran/Takai combination, each combining the currents from the respective two adjacent reference cells to establish one of the

reference levels of Naji, for the purpose of providing stable and reliable reference levels for multilevel magnetic random access memories that better track with the characteristics of the memory cells and therefore reducing the effects of manufacturing variations, noise, temperature, etc. (see for example Tran column 4, lines 44-63).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Perner et al. (U.S. Pat. No. 6,324,093), Perner et al. (U.S. Pat. No. 6,501,697), Perner et al. (U.S. Pat. No. 6,456,524), Perner (U.S. Pat. No. 6,256,247), Thewes et al. (U.S. Pat. No. 6,490,192) and Sugibayashi et al. (U.S. Pat. No. 6,678,187) discloses an MRAM sensing circuit with a current mirror.

Zhu et al. (U.S. Pat. No. 5,768,181), Chen et al. (U.S. Pat. No. 5,917,749) and Chen et al. (U.S. Pat. No. 5,953,248) discloses a multi-state MRAM.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800